IN THE CLAIMS

Following are the claims as currently pending for consideration.

1. (Original) An apparatus for accessing data in a memory, the apparatus comprising:

a bit vector replacement circuit to receive a first bit vector and a control signal and to substitute a constant bit vector for the first bit vector, in response to the control signal being in a first state, to produce a second bit vector;

a pre-decoder coupled with the bit vector replacement circuit to receive a plurality of bit vectors including the second bit vector, to combine subsequences from the plurality of bit vectors to identify possible wordline subsequences corresponding to the plurality of bit vectors, and to activate a subsequence indicator for an identified possible wordline subsequence; and

a wordline decoder coupled with the pre-decoder to combine activated subsequence indicators to identify a unique wordline corresponding to the plurality of bit vectors.

2. (Original) The apparatus of Claim 1, wherein the plurality of bit vectors correspond to an address represented in carry-sum redundant form.

3. (Original) The apparatus of Claim 1, wherein the plurality of bit vectors comprise:

a carry bit vector including a carry bit corresponding to a binary digit of the address; and

a sum bit vector including a sum bit corresponding to a binary digit of the address.

4. (Original) The apparatus of Claim 3, wherein the first bit vector is the carry bit vector.

5. (Original) The apparatus of Claim 4, wherein the second bit vector produced by the bit vector replacement circuit in response to the control signal being in a second state corresponds to the carry bit vector.

6. (Original) The apparatus of Claim 1, wherein the plurality of bit vectors correspond to an address represented in sign-digit redundant form.

7. (Original) The apparatus of Claim 6, wherein the plurality of bit vectors comprise:

a sign bit vector including a sign bit corresponding to a binary digit of the address; and

a magnitude bit vector including a magnitude bit corresponding to a binary digit of the address.

8. (Original) The apparatus of Claim 7, wherein the first bit vector is the sign bit vector.

9. (Original) The apparatus of Claim 8, wherein the second bit vector produced by the bit vector replacement circuit in response to the control signal being in a second state corresponds to the sign bit vector.

10. (Original) The apparatus of Claim 1, wherein the vector replacement circuit substitutes a constant bit vector corresponding to a zero vector for the first bit vector.

11. (Original) The apparatus of Claim 1, wherein the pre-decoder is a carry nonpropagative circuit.

12. (Original) The apparatus of Claim 11, wherein the pre-decoder identifies possible two-bit wordline subsequences.

13. (Original) The apparatus of Claim 11, wherein the pre-decoder activates a subsequence indicator for an identified possible two-bit subsequence.

14. (Original) The apparatus of Claim 1, wherein one of the plurality of bit vectors corresponds to an address represented in unsigned binary form.

15. (Original) The apparatus of Claim 14, wherein said one of the plurality of bit vectors corresponds to a store address.

16. (Original) The apparatus of Claim 1, further comprising:

a cache coupled with the wordline decoder to store a copy of a datum stored in the memory, the copy being stored at a wordline in the cache corresponding to an address in the memory.

17. (Original) The apparatus of Claim 16, further comprising:

a processor coupled with the pre-decoder to produce the plurality of bit vectors.

18. (Original) The apparatus of Claim 17, wherein the processor produces one or more of the plurality of bit vectors by adding together addressing components including a base address and an index or a displacement.

19. (Original) A digital computing system comprising:

a die;

a bit vector selection circuit on the die to receive a first bit vector and a control signal, and to select a constant bit vector or the first bit vector responsive to the control signal, and to output the selected bit vector as a second bit vector;

a decoder circuit on the die coupled to the bit vector selection circuit to receive a plurality of bit vectors including the second bit vector and to combine a subsequence from each of the plurality of bit vectors to identify a wordline corresponding to the plurality of bit vectors;

an internal cache on the die, the internal cache coupled with the decoder circuit to store a first datum at the wordline corresponding to the plurality of bit vectors;

a processor on the die coupled with the decoder circuit to produce the plurality of bit vectors; and

an external cache, not on the die, to store a second datum, the external cache coupled with the die and with the internal cache, to transmit the second datum to the internal cache to be stored on the die.

20. (Original) The digital computing system of Claim 19, wherein the plurality of bit vectors correspond to an address represented in carry-sum redundant form and the plurality of bit vectors comprise:

a carry bit vector including a carry bit corresponding to a binary digit of the address; and

a sum bit vector including a sum bit corresponding to a binary digit of the address.

21. (Original) The digital computing system of Claim 20, wherein the first bit vector is the carry bit vector.

22. (Original) The digital computing system of Claim 19, wherein one of the plurality of bit vectors corresponds to an address represented in unsigned binary form.

23. (Original) The apparatus of Claim 22, wherein said one of the plurality of bit vectors corresponds to a store address.

24. (Original) A cache memory system comprising:

a plurality of lines for storing copies of memory storage locations having corresponding addresses;

means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in a redundant form; and

means for decoding an address to access a line of the cache memory system responsive to an access request that includes an address represented in unsigned binary form.

25. (Currently Amended) A method of accessing data in a first storage, the method comprising:

copying a plurality of storage locations from a second storage into a plurality of wordlines of the first storage by asserting corresponding wordline signals;

receiving an access request including a first bit vector, a second bit vector and a control signal;

setting the second bit vector equal to a constant bit vector if the control signal is in a first state;

identifying at least in part from the second bit vector and from the first bit vector a word line corresponding to the combined first bit vector and second bit vector[[:]];

asserting the identified wordline signal; and

accessing the wordline of the first storage corresponding to the assertedword line signal.

26. (New) The method of Claim 25, wherein the second bit vector is a carry bit vector.

27. (New) The method of Claim 26, wherein said one of the plurality of bit vectors corresponds to a store address.

28. (New) The method of Claim 25, wherein the first bit vector corresponds to an address represented in unsigned binary form.

29. (New) The cache memory system of Claim 24, wherein the address represented in a redundant form comprises a first bit vector that is a sign bit vector.

30. (Original) The cache memory system of Claim 29, wherein decoding an address to access a line of the cache memory system responsive to the access request comprises producing a second bit vector corresponding to the sign bit vector.

31. (Original) The cache memory system of Claim 24 further comprising a pre-decoder that is a carry nonpropagative circuit.

32. (Original) The cache memory system of Claim 31, wherein the pre-decoder identifies possible two-bit wordline subsequences.

33. (Original) The The cache memory system of Claim 31, wherein the pre-decoder activates a subsequence indicator for an identified possible two-bit subsequence.